What is claimed is:

1. A resistor comprising:

a substrate having first and second opposite flat surfaces and having a shape and a composition;

a first resistive foil having a low TCR of about 0.1 to about 1 ppm/°C and a thickness of about 0.03 mils to about 0.7 mils cemented to the first flat surface with a cement;

the first resistive foil having a pattern to produce a desired resistance value;

the substrate having a modulus of elasticity of about 10×10^6 psi to about 100×10^6 psi and a thickness of about 0.5 mils to about 200 mils;

the first resistive foil, pattern, and substrate being selected to provide a cumulative effect of reduction of resistance change due to power.

2. The resistor of claim 1 wherein the shape of the substrate is selected to provide the cumulative effect of reduction of resistance change due to power.

3. The resistor of claim 1 wherein the composition of the substrate is selected to provide the cumulative effect of reduction of resistance change due to power.

4. The resistor of claim 1 wherein the thickness of the substrate is selected to provide the cumulative effect of reduction of resistance change due to power.

5. The resistor of claim 1 wherein the TCR of the first resistive foil is selected to provide the cumulative effect of reduction of resistance change due to power.

6. The resistor of claim 5 wherein the first resistive foil is etched to form longitudinal and transverse strands in a pattern selected to reduce bending and provide the cumulative effect of reduction of resistance change due to applied power.

7. The resistor of claim 1 wherein the cement is selected to provide the cumulative to reduce the effect of resistance change due to power.

8. The resistor of claim 6 wherein the heat transmissivity of the cement is selected to provide the cumulative effect of reduction of resistance change due to power.

9. The resistor of claim 6 wherein the thickness of the cement is selected to provide the cumulative effect of reduction of resistance change due to power.

10. The resistor of claim 1 further comprising a second resistive foil having a low TCR of about 0.1 to about 1 ppm/°C and a thickness of about 0.03 mils to about 0.7 mils cemented to the second flat surface, the second resistive foil connected to the first resistive foil, the first resistive foil and second resistive foil having approximately equal resistance values and providing approximately equal power dissipation on both surfaces of the substrate thereby reducing temperature gradients across the substrate, preventing bending of the substrate, and avoiding resistance change associated with bending.

11. The method of claim 10 further comprising cementing a second resistive foil having a low TCR of about 0.1 to about 1 ppm/°C and a thickness of about 0.03 mils to about 0.7 mils to a second surface of the substrate opposite the first surface, the first and second resistive foils patterned to have approximately equal resistance value.

12. The method of claim 11 further comprising interconnecting the first resistive foil and the second resistive foil to provide approximately equal power dissipation on the first and second surfaces thereby reducing temperature gradients across the substrate, preventing bending of the substrate, and avoiding resistance change due to bending.

13. A method of manufacturing a low power coefficient resistor comprising:

cementing a first resistive foil and a second resistive foil on opposite surfaces of a substrate;

the first and second resistive foils patterned to have approximately equal resistance values;

interconnecting the first and second resistive foils to provide approximately equal power dissipation on the substrate;

thereby reducing temperature gradients across the substrate, preventing bending of the substrate and avoiding resistance change due to bending of the substrate.